In the Claims:

1. (Original) A semiconductor device, comprising:

an on-chip termination circuit that is configured to generate a variable resistance to an input signal based on at least one code signal;

a reference voltage generator that is configured to generate a reference voltage based on the at least one code signal; and

an input buffer that is configured to generate an internal signal based on the input signal from the on-chip terminal circuit and the reference voltage.

2. (Original) The semiconductor device of Claim 1, wherein the at least one code signal comprises a pull-up code signal and a pull-down code signal, and wherein the on-chip termination circuit comprises:

a pull-up termination resistor that is configured to have a variable resistance based on the pull-up code signal; and

a pull-down termination resistor that is configured to have a variable resistance based on the pull-down code signal, wherein the pull-up termination resistor and the pull-down termination resistor are connected in series between a first power supply voltage and a second power supply voltage, and wherein the input signal is conducted through a connection node between the pull-up termination resistor and the pull-down termination resistor.

3. (Original) The semiconductor device of Claim 2, wherein the reference voltage generator comprises:

a first resistor that is configured to have a variable resistance based on the pull-up code signal; and

a second resistor that is configured to have a variable resistance based on the pull-down code signal, wherein the first and second resistors are connected in series between the first power supply voltage and the second power supply voltage, and wherein the reference voltage is generated at a node between the first and second resistors.

4. (Original) The semiconductor device of Claim 3, wherein:

the pull-up termination resistor has the same variable resistance based on the pull-up code signal as the first resistor; and

the pull-down termination resistor has the same variable resistance based on the pull-down code signal as the second resistor.

5. (Original) The semiconductor device of Claim 2, further comprising a calibration circuit that is configured to generate the pull-up code signal and the pull-down code signal based on resistance of an external resistor that is external to the semiconductor device.

6. (Original) The semiconductor device of Claim 1, wherein the on-chip termination circuit comprises a termination resistor that is configured to generate a variable resistance to the input signal based on a first code signal.

7. (Original) The semiconductor device of Claim 6, wherein the termination resistor is connected between a power supply voltage and a node through which the input signal is conducted to the input buffer.

8. (Original) The semiconductor device of Claim 1, wherein the reference voltage generator is configured to generate the reference voltage based on an external reference voltage signal that is received from external to the semiconductor device.

9. (Original) The semiconductor device of Claim 1, further comprising:

a plurality of input pins, wherein each of the input pins is configured to receive a different input signal;

a plurality of the on-chip termination circuits, wherein each of the on-chip termination circuits is coupled to a different one of the input pins and is configured to generate a variable resistance to a respective one of the input signals from the input pins based on different ones of a plurality of code signals;

a plurality of the reference voltage generators, wherein each of the reference voltage generators is paired with at least one of the plurality of the on-chip termination circuits, and is configured to generate a reference voltage based on the same one of the plurality of code signals as the paired on-chip termination circuit; and

a plurality of input buffers, wherein each of the input buffers is configured to receive the input signal and the reference voltage from a different pair of the on-chip termination circuits and the reference voltage generators, and is configured to convert the received input signal into an internal signal.

10. (Canceled).

11. (Canceled).

12. (Currently amended) A semiconductor device, comprising:

an input pin that is configured to receive an input signal from external to the semiconductor device;

an on-chip termination circuit that comprises a pull-up termination resistor and a pull-down termination resistor, wherein the pull-up termination resistor and the pull-down termination resistor are connected in series between a first power supply voltage and a second power supply voltage, and wherein the input signal is conducted through a connection node between the pull-up termination resistor and the pull-down termination resistor;

a reference voltage generator that comprises a first resistor and a second resistor, wherein the first and second resistors are connected in series between the first power supply voltage and the second power supply voltage, and wherein the reference voltage is generated at a node between the first and second resistors; and

an input buffer that is configured to generate an internal signal based on the input signal from the on-chip terminal circuit and the reference voltage, wherein:

the pull-up termination resistor has the same resistance as the first resistor;

the pull-down termination resistor has the same resistance as the second resistor;

~~The semiconductor device of Claim 11, wherein:~~

the pull-up termination resistor is configured to have a variable resistance based on a pull-up code signal;

the first resistor is configured is configured to have a variable resistance based on the pull-up code signal;

the pull-down termination resistor is configured to have a variable resistance based on a pull-down code signal; and

the second resistor is configured to have a variable resistance based on a pull-down code signal.

13. (Original) The semiconductor device of Claim 12, wherein:

the pull-up termination resistor and the first resistor are configured to have the same variable resistance based on the pull-up code signal; and

the pull-down termination resistor and the second resistor are configured to have the same variable resistance based on the pull-down code signal.

14. (Original) The semiconductor device of Claim 12, further comprising a calibration circuit that is configured to generate the pull-up code signal and the pull-down code signal based on resistance of an external resistor that is external to the semiconductor device.

15. (Canceled).

16. (Original) A semiconductor device, comprising:

an on-chip termination circuit that is configured to generate a variable resistance to an input signal based on a first code signal, wherein the on-chip terminal circuit comprises a termination resistor that is configured to generate the variable resistance to the input signal based on the first code signal;

a reference voltage generator that is configured to generate a reference voltage based on a second code signal, wherein the reference voltage generator comprises a first resistor that is configured to have a variable resistance based on the second code signal, and a second

resistor that is configured to have a variable resistance based on the second code signal, wherein the first and second resistors are connected in series between a first power supply voltage and a second power supply voltage, and wherein the reference voltage is generated at a node between the first and second resistors; and

an input buffer that is configured to generate an internal signal based on the input signal from the on-chip terminal circuit and based on the reference voltage.

17. (Original) The semiconductor device of Claim 16, wherein the termination resistor is connected between the first power supply voltage and a node through which the input signal is conducted to the input buffer.

18. (Original) The semiconductor device of Claim 16, wherein the termination resistor has a resistance that is about the same as the total resistance of the first resistor and the second resistor.

19. (Original) The semiconductor device of claim 16, further comprising a calibration circuit that is configured to generate the first code signal and the second code signal so that the termination resistor has twice the resistance as the first resistor and the second resistor.

20. (Original) The semiconductor device of Claim 16, further comprising a calibration circuit that is configured to generate the first code signal and the second code signal based on resistance of an external resistor that is external to the semiconductor device.

21. (Original) The semiconductor device of Claim 16, wherein the reference voltage generator further comprises a reference voltage driver connected in series between the second supply voltage and both of the first and second resistors.

22. (Original) The semiconductor device of Claim 16, further comprising:

an input pin through which the input signal is received from external to the semiconductor device; and

a pull-down driver which is connected between the input pin and the second power supply voltage.